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PATENT  
Attorney Docket No. ASC-049C1  
(120237/156689)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT: Fitzgerald  
 SERIAL NO.: 10/774,890 GROUP NO.: 2818  
 FILING DATE: February 9, 2004 EXAMINER: Tran, Mai Huong C.  
 TITLE: RELAXED SiGe PLATFORM FOR HIGH SPEED CMOS  
 ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS

Mail Stop RCE  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicant hereby makes of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the non-patent publications are enclosed.

**REMARKS**

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or

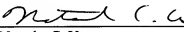
Supplemental Information Disclosure Statement  
Serial No. 10/774,890  
Page 2 of 2

- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.


It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Respectfully submitted,

Date: Feb. 17, 2006  
Reg. No. 44,381

  
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FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT				ATTORNEY DOCKET NO.: ASC-049C1			
				APPLICANT:		Fitzgerald	
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U.S. PATENT DOCUMENTS							
EXAM. INT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A191	5,091,767	02/25/1992	Bean et al.			
	A192	5,571,373	11/05/1996	Krishna et al.			
	A193	5,633,202	05/27/1997	Brigham et al.			
	A194	5,710,450	01/20/1998	Chau et al.			
	A195	5,976,939	11/02/1999	Thompson et al.			
	A196	6,876,053	04/05/2005	Ma et al.			
OTHER ART, JOURNAL ARTICLES, ETC.							
EXAM. INT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)						
	C135	Abstreiter et al., "Silicon/Germanium Strained Layer Superlattices," <u>Journal of Crystal Growth</u> , 95:431-438 (1989).					
	C136	Auberton-Hervé et al., "SMART-CUT®: The Basic Fabrication Process for UNIBOND® SOI Wafers," <u>IEICE Transactions on Electronics</u> , E80-C(3):358-363 (1997).					
	C137	Cao et al., "0.18- $\mu$ m Fully-Depleted Silicon-on -Insulator MOSFET's," <u>IEEE Electron Device Letters</u> , 18(6):251-253 (1997).					
	C138	Chau et al., "Advanced CMOS Transistors in the Nanotechnology Era for High-Performance, Low-Power Logic Applications", pp. 26-30 (2004).					
	C139	Eichinger et al., "Characterization of MBE Growth SiGe Superlattices with SIMS and RBS, <u>Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy</u> , 85(7):367-375 (1985).					
	C140	Fair, "Concentration Profiles of Diffused Dopants in Silicon," <u>Impurity Doping Processes in Silicon</u> , Chapt. 7, pp. 318-442 (1981).					
	C141	Fair, "Quantified Conditions for Emitter-Misfit Dislocation Formation in Silicon," <u>Journal of the Electrochemical Society</u> , 125(6):923-926 (1978).					
	C142	Fathy et al., "Formation of epitaxial layers of Ge on Si substrates by Ge implantation and oxidation", <u>Appl. Phys. Lett.</u> , 51(17):1337-1339 (1987).					
	C143	Ghani et al., "Effect of oxygen on minority-carrier lifetime and recombination currents in Si <sub>1-x</sub> Ge <sub>x</sub> heterostructure devices", <u>Appl. Phys. Lett.</u> , 58(12):1317-1319 (1991).					
EXAMINER		/Dung A. Le/ (08/01/2008)			DATE CONSIDERED		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Die/ (08/01/2008)

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OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C144	Gibbons et al., "Limited reaction processing: Silicon epitaxy", <u>Appl. Phys. Lett.</u> , 47(7):721-723 (1985).
	C145	Godbey et al., "A Si <sub>0.7</sub> Ge <sub>0.3</sub> Strained Layer Etch Stop for the Generation of Bond and Etch Back SOI", <u>IEEE SOS/SOI Tech. Conf. Proc.</u> , p. 143-144 (1989).
	C146	Gronet et al., "Growth of GeSi/Si strained-layer superlattices using limited reaction processing", <u>J. Appl. Phys.</u> , 61(6):2407-2409 (1987).
	C147	Hobart et al., "Ultra-Cut: A Simple Technique for the Fabrication of SOI Substrates with Ultra-Thin (<5 nm) Silicon Films," <u>Proceedings 1998 IEEE International SOI Conference</u> , pp. 145-146 (1998).
	C148	Holländer et al., "Reduction of Dislocation Density of MBE-Grown Si <sub>1-x</sub> Ge <sub>x</sub> Layers on (100) Si by Rapid Thermal Annealing", <u>Thin Solid Films</u> , 183:157-164 (1989).
	C149	Huang et al., "SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors", <u>Appl. Phys. Lett.</u> , 78(9):1267-1269 (2001).
	C150	Hull et al., "Structural Studies of GeSi/Si Heterostructures", <u>Proceedings of the First International Symposium on Silicon Molecular Beam Epitaxy</u> , 85(7): 376-384 (1985).
	C151	Ismail, et al., "Extremely high electron mobility in Si/SiGe modulation-doped heterostructures", <u>Appl. Phys. Lett.</u> , 66(9):1077-1079 (1995).
	C152	Ismail, et al., "Gated Hall effect measurements in high-mobility n-type Si/SiGe modulation-doped heterostructures", <u>Appl. Phys. Lett.</u> , 66(7):842-844 (1995).
	C153	Ismail, et al., "Identification of a Mobility-Limiting Scattering Mechanism in Modulation-Doped Si/SiGe Heterostructures", <u>Physical Review Letters</u> , 73(25):3447-3452 (1994).
	C154	Kasper, "Growth and Properties of Si/SiGe Superlattices", <u>Surface Science</u> , 174:630-639 (1986).
	C155	Maleville et al., "Physical Phenomena Involved in the Smart-Cut® Process", <u>Electrochemical Society Proceedings</u> , 96(3):34-46 (1996).
	C156	Mistry et al., "Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology," <u>Symposium on VLSI Technology Digest of Technical Papers</u> , pp. 50-51 (2004).
	C157	Monroe et al., "Comparison of mobility-limiting mechanisms in high-mobility Si <sub>1-x</sub> Ge <sub>x</sub> heterostructures", <u>J. Vac. Sci. Technol. B</u> , 11(4):1731-1737 (1993).
	C158	Noble et al., "Reduction in misfit dislocation density by the selective growth of Si <sub>1-x</sub> Ge <sub>x</sub> /Si in small areas", <u>Appl. Phys. Lett.</u> , 56(1):51-53 (1990).
EXAMINER	/Dung A. Le/ (08/01/2008)	
	DATE CONSIDERED	

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